REMARKS

Claims 1-20 are presented for further examination. Claim 1, 2, 5-7, 10-12, and 15-17 have been amended. Claims 19-20 are new.

In the Office Action mailed April 11, 2003, the Examiner objected to the claims because reference characters corresponding to elements recited in the detailed description appeared in the claims without being enclosed in parentheses. Applicant has reviewed the claims and can find no such reference numbers appearing therein. However, applicant has amended claims 5 and 6 so that the numerals used therein are now written out in text format. These numerals, however, were not reference numbers that referred to elements in the drawings.

Claims 1-6 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite because "the read mode" at line 8 in claim 1 had insufficient antecedent basis. Claim 1 has been amended to overcome this rejection.

Claims 1-4 and 7-17 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,414,701 ("Shtayer"). Claims 5, 6, and 18 were objected to but found to be allowable if rewritten into independent form.

Applicant respectfully disagrees with the basis for the rejection and requests reconsideration and further examination of the claims.

The present invention as disclosed and claimed in the application is directed to associating indexes to addresses that are chosen from a larger number of addresses. Each index is stored in a memory that also includes an enabling bit and an associated check word. The index and the check word correspond to predetermined bits of an address associated with the index. When an address is received, some of the bits of the received address are used as a "packed address" to point to the memory. The remaining bits are compared to the check word stored in the memory. When the remaining bits match the check word stored in the memory, the respective index is then associated with the received address.

Shtayer teaches a method and data structure for performing address compression in an asynchronous transfer mode (ATM) system. The Examiner asserts that "Shtayer discloses a device . . . including tables (a memory) containing VPI's (indexes) and VP Pointers (respective check words) corresponding to predetermined bits of the addresses associated with the indexes

(Fig. 3, column 2, lines 20-43, column 5, lines 30-column 6, lines 5) . . . ." Applicant respectfully disagrees with this analysis.

More particularly, as shown by reference numeral 26 in Figure 3 of Shtayer, the VPI is only used in combination with a VP mask to create a VPI-based index (see col. 5, lines 64-68). The VPIs are not stored in a table. They are used to address the table 22a. The VPI therefore cannot be considered as indexes stored in a memory as in the present invention.

Moreover, the VP Pointers (see col. 5, lines 58-61 of Shtayer) are pointers used to address the beginning of table 22a. Shtayer does not suggest that these can correspond to predetermined bits of an address. The VP Pointers of Shtayer can therefore not be considered as "check words" according to the disclosed and claimed embodiments of the present invention.

The Examiner further asserts that Shtayer discloses "compressing . . . a current address and suppressing in this address bits determined by a pattern such that the suppressed bits correspond to bits of the VP mask (check words) . . . ." Applicant respectfully disagrees with this analysis.

Examples of VP masks are given by Shtayer at column 6, lines 50-68, which show clearly that a VP mask is used to extract predetermined bits of an address. More particularly, Shtayer teaches using a value of one for each bit to be extracted. Therefore, Shtayer does not correspond to predetermined bits of the address because it contains no information about the value of the extract bits. The VP masks can therefore not be considered as check words in accordance with the disclosed and claimed embodiments of the present invention.

More particularly, Shtayer teaches at column 6, lines 50-68, that compressing of the address consists in keeping the address bits that are determined by a pattern, which is the logical combining of a VPI/VCI address and a VP/VC mask. This does not correspond to suppressing the bits as disclosed and claimed in the present invention. Thus, Shtayer's teaching of address compressing of the VP Pointers is not related to the address packing of the present invention.

The Examiner also states that Shtayer discloses "indicating that the current address corresponds to the selected table location (memory location) if the bits of the VP offset

(check words) of the selected location are valid (equal to the) corresponding to bits of the current address (column 6, lines 19-50) . . . ." Applicant respectfully disagrees with this analysis.

Applicant can find no teaching or suggestion in Shtayer of a "VP offset." Rather, Shtayer teaches at column 6, lines 23-28, a VC offset, which is added to a VC Pointer to find a particular subtable. This does not teach or suggest predetermined bits of any address. The VC offsets, therefore, cannot be considered as "check words" in accordance with the disclosed and claimed embodiments of the present invention.

Turning to the claims, claim 1 is directed to a device for associating indexes to addresses chosen from a greater number of addresses than the number of available indexes. The device includes a memory containing indexes and respective check words corresponding to predetermined bits of the addresses associated with the indexes. Nowhere does Shtayer teach or describe the use of indexes and respective check words nor the storing of such indexes and respective check words in a memory.

Claim 1 further recites a packing circuit receiving a current address and suppressing in this current address bits determined by a pattern such that the suppressed bits correspond to bits of the check words, the packed addressed provided by the packing circuit used to select in a read mode a memory location. Nowhere does Shtayer teach or suggest suppressing bits from the current address and using the suppressed bits to correspond to the check words stored in the memory.

Claim 1 further recites a comparator indicating that the current address corresponds to the selected memory location when the bits of the check words of the selected location are equal to the corresponding bits of the current address. Nowhere does Shtayer teach or suggest using some of the bits of the received address as a packed address to point to the memory or comparing the remaining bits therefrom to the check words stored in the memory.

In view of the foregoing, applicant respectfully submits that claim 1 as well as dependent claims 2-6 are clearly in condition for allowance.

Independent claim 7 recites an address association device that comprises a masking circuit, packing circuit, memory, and comparator having the functions essentially as recited in claim 1, and wherein the masking circuit is also included to recite receiving a plurality

of address bits and masking the address bits in accordance with a predetermined mask pattern. Claim 7 further recites the packing circuit suppressing a plurality of check words from the address bits and the memory configured to receive and associate the index bits and check word bits with the bits located therein. Applicant respectfully submits that claim 7 and dependent claims 8-11 are allowable for the reasons discussed above with respect to claim 1.

Independent claim 12 is a method claim that recites the steps of receiving and masking the plurality of address bits, packing the masked plurality of addressed bits to reduce the number of address bits according to a predetermined packing pattern, and suppressing check word bits from the masked address bits; associating the packed address bits with a memory location corresponding to a network location; and comparing selected bits from the plurality of address bits for a selected memory location with selected bits associated with a memory location addressed in the plurality of address bits and indicating when there is a match. Nowhere does Shtayer teach or suggest that combination of steps recited in method claim 12. Applicant respectfully submits that claim 12 and dependent claims 13-18 are allowable.

New claims 19 and 20 correspond to allowable dependent claims 5 and 6. More particularly, the allowable subject matter of claim 5 has been incorporated into claim 1 to now become independent claim 19. The subject matter of claim 6 has been combined with the subject matter of claim 19 to become claim 20. Applicant respectfully submits that claims 19 and 20 are allowable inasmuch as claims 5 and 6 have been found to be allowable.

In view of the foregoing, applicant respectfully submits that all of the claims remaining in this application are now in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

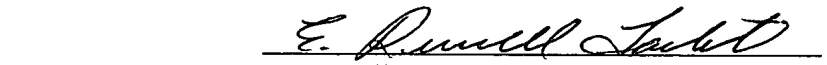
Applicant is submitting herewith substitute formal drawings for Figures 1 and 2 wherein the legend "Prior Art" has been added. No new matter has been added. Approval and entry of the substitute formal drawings is respectfully requested.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

Pascal Moniot

SEED Intellectual Property Law Group PLLC



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